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QUESTION BANK (DESCRIPTIVE)

Subject with Code :DSD(18EC0402) **Course & Branch**: B.Tech - ECE

Year & Sem: II B.Tech & I Sem **Regulation:** R18

UNIT –I

Essay Answer (10 mark) Questions

1. (a) Convert the given decimal number 234 to binary, octal, hexadecimal and BCD equivalent. **[6M][L1][CO1]**
   (b) Given that $(16)_{10} = (100)_b$, determine the value of b. **[2M][L1][CO1]**
   (c) Given that $(292)_{10} = (1204)_b$, determine the value of b. **[2M][L1][CO1]**
2. (a) Convert the following. **[5M][L1][CO1]**
   i) $(BC)_{16} = (\ )_{10}$ ii) $(2314)_8 = (\ )_{10}$ iii) $(1000011)_2 = (\ )_{10}$ iv) $(647)_{10} = (\ )_{16}$
   (b) Express the following numbers in decimal. **[3M][L1][CO1]**
   i) $(10110.0101)_2$ ii) $(16.5)_{16}$ iii) $(26.24)_8$
   (c) Convert decimal 27.315 to binary. **[2M][L1][CO1]**
3. Perform the following
   (a) Subtraction using 9's complement for the given. **[5M][L1][CO1]**
   i) 54321 –41245 ii) 1231-4145
   (b) Subtraction by using 1's complement for the given. **[5M][L1][CO1]**
   i) 111011-110110 ii) 10001-10011
4. Perform the following
   (a)Subtraction using 10's complement for the given. **[5M][L1][CO1]**
   i) 3456 – 245 ii) 1631-745
   (b) Subtraction by using 2's complement for the given. **[5M][L1][CO1]**
   i) 111001-1010 ii) 10011-10001
5. (a) Perform the following using BCD arithmetic. **[5M][L1][CO1]**
   i) $(79)_{10} + (177)_{10}$ ii) $(481)_{10} + (178)_{10}$
   (b) Convert the following to binary and then to gray code. **[5M][L1][CO1]**
   i) $(1111)_{16}$ ii) $(BC54)_{16}$ iii) $(237)_8$ iv) $(164)_{10}$ v) $(323)_8$
6. (a) Explain about the Binary Codes. **[5M][L1][CO1]**
   (b)Simplify the following Boolean functions to minimum number of literals. **[5M][L1][CO1]**
   i) F=xy+x'z+yz.
   ii) F=x'y'z+x'yz+xy'
   iii) F= (x+y)'(x'+y')
   iv) F=xy+xy'+x'y
   v) F= (BC'+A'D)(AB'+CD')
7. (a) State and prove De Morgan's theorem. **[4M][L1][CO1]**
   (b) State and prove Duality theorem. **[4M][L1][CO1]**
   (c) State the distributive law. **[2M][L1][CO1]**
8. (a) Obtain the Dual and complement to the following Boolean expressions. **[8M][L1][CO1]**
   i) F=AB+A (B+C) + B' (B+D)
   ii) F=A+B+A'B'C
   iii)F=A'B+A'BC'+A'BCD+A'BC'D'E

iv) F= ABEF+ABE'F'+A'B'EF

(b)Give the truth table of XNOR logic gates. **[2M][L1][CO1]**

9. (i) Express the Boolean function F= A+B'C as a sum of minterms. **[5M][L1][CO1]**
   (ii) Express the Boolean function F= XY+X'Z as a product of maxterm. **[5M][L1][CO1]**
10. (a)Express the following function as a sum of minterms and as a product of maxterms
    F(A,B,C,D) = B'D+A'D+BD. **[5M][L1][CO1]**
    (b)Obtain the truth table of the following Boolean function and express the function as sum of minterms and product of maxterms F = (A+B) (B+C). **[5M][L1][CO1]**

UNIT –II
Essay (10 mark) Questions

1. a) Minimize the following Boolean function using K-map
   F (A, B, C, D)= Σm(1,4,5,6,12,13,14,15). **[2M][L1][CO3]**
   b) Obtain the simplified expression using K-map for the following Boolean function
   F (A, B, C, D, E) =∑ (0,1,4,5,16,17,21,25,29). **[3M][L1][CO3]**
   c) Simplify F(A,B,C,D) = ∑ (4,5,6,7,12,13,14) +d(1,9,11,15) using K-map. **[5M][L1][CO3]**
2. Simplify the following Boolean function for minimal SOP & POS form using K-map
   i) F (A, B, C, D) = Σ (0,1,2,5,8,9,10)
   ii) F (A, B, C, D) = π(1,3,5,7,12,13,14,15). **[10M][L2][CO3]**
3. Obtain (i) Sum of products form and (ii) Product of sums form for
   F=x'z'+y'z'+yz'+xy **[10M][L2][CO3]**
4. Minimize the given Boolean function, F (A, B,C,D) = Σ m(0,1,2,3,6,7,13,15) using Tabulation method and implement it using basic gates. **[10M][L2][CO3]**
5. (a)Write the design procedure for combinational circuit. **[5M][L3][CO4]**
   (b) Design & implement the Full Adder . **[5M][L3][CO4]**
6. (a) Design & implement 4-bit Adder/subtractor. **[4M][L3][CO4]**
   (b) Explain about carry look ahead adder with suitable diagram. **[6M]L1][CO4]**
7. (a) Construct a BCD adder circuit**.** [**3M][L3][CO4]**
   (b)With a neat design procedure, explain the implementation of a 4-bit Magnitude Comparator. **[7M][L3][CO4]**
8. (a) Define Decoder. Design & implement a 3 to 8 line Decoder**.** **[5M][L3][CO4]**
   (b) Design & implement a Full Adder using Decoder and two OR gates. [**5M][L3][CO4]**
9. (a) What is Encoder? Design an octal to binary Encoder. **[5M][L3][CO4]**
   (b) Design & Implement an 8:1 Multiplexer. **[5M][L3][CO4]**
10. (a) Implement the following Boolean function using 4:1 Multiplexer.
    F (A, B, C) =∑ (1,2,6,7). **[5M][L3][CO4]**
    (b) Design a 1:4 Demultiplexer and mention the applications of a DEMUX. **[5M][L1][CO4]**

UNIT –III
Essay (10 mark) Questions

1. (a) Draw the logic diagram of a JK – flip flop and explain its operation. **[5M][L4][CO3]**
   (b) What is the need for Master Slave JK FF and explain its operation with neat diagrams. **[5M][L2][CO3]**
2. (a)Explain the operation of an SR Flip Flop using excitation table. Give its Truth Table and Characteristic Equation **[5M][L2][CO3]**
   (b)Give the characteristic table, Truth table, characteristic equation and excitation table for T and DFF. **[5M][L2][CO3]**
3. (a)Implement D-FF using JK FF with its truth table. **[5M][L4][CO3]**
   (b) Draw the basic flip flop circuit with NOR gates. Explain its operation **[5M][L2][CO3]**
4. (a)Compare Synchronous and Ripple counters. **[3M][L2][CO2]**
   (b) Design and implement Mod-10 Synchronous Up counter using T-FFs **[7M][L4][CO3]**
5. (a)Design MOD -6 Ripple Down counter **[5M][L4][CO3**
   (b)Draw and explain a 4-bit Serial in Serial out (SISO) Shift Register. **[5M][L4][CO3]**
6. Draw and explain 4-bit Universal shift register. **[10M][L6][CO3]**
7. (a)Explain the difference between Ring and Johnson counters with neat sketch. **[5M][L4][CO3]**
   (b) Design a 4-bit synchronous up counter using JK flip flops. **[5M][L2][CO4]**
8. (a) Design a Positive edge triggered Master-Slave D flip flop **[4M][L2][CO3]**
   (b) Design and implement a BCD Ripple counter using JK Flip Flops. **[6M][L3][CO3]**
9. (a)Design a 4-bit binary ripple down – counter using a negative edge triggered T – Flip Flops. **[5M][L3][CO3]**
   (b)Explain the operation of Pseudo Random Binary Sequence Generator with a neat diagram. **[5M][L2][CO3]**
10. (a)Explain the principle of clock generation with neat diagram **[4M][L4][CO3]**
    (b) Design and implement a 2 bit Up-Down Counter using JK FF's. [**6M][L4][CO3]**

UNIT –IV
Essay (10 mark) Questions

1. (a)Perform the analysis of standard DTL NAND gate and give its characteristics **[5M][L4][CO3]**
   (b)Give the classification of integrated circuits and compare the various logic families. **[5M][L2][CO2]**
2. (a)What is meant by Tristate logic? Draw the circuit of Tristate TTL logic and explain the functions. **[6M][L4][CO4]**
   (b)Explain the following specifications **[4M][L2][CO2]**
   (i) Fan out
   (ii)Noise margin
3. (a) Briefly Explain about ECL. **[5M][L2][CO2]**
   (b) Compare between Different CMOS Logic families. **[5M][L1][CO2]**
4. (a)Explain about TTL to CMOS interfacing **[5M][L4][CO2]**
   (b)Compare TTL, ECL and CMOS **[5M][L1][CO2]**
5. Design a BCD to excess 3 code converter using suitable PLA **[10M][L4][CO4]**
6. Implement the following functions using a PLA ` **[10M][L4][CO3]**
   (i)f1(w,x,y)=∑m(3,5,6,7) ii) f2(w,x,y)=∑m(0,2,4,7)
7. Generate the following Boolean function using PAL with 4 inputs and 4 outputs **[10M][L6][CO3]**
   (i)Y3= a'bc'd+a'bcd'+abc'd
   (ii)Y2=a'bcd'+a'bcd+abcd
   (iii)Y1=a'bc'+a'bc+ab'c+abc'
   (iv)Y0=abcd8.
8. (a)Derive the PLA programming table for the combinational circuit that squares a 3-bit number. **[5M][L2][CO4]**
   (b) Compare three combinational circuits: PLA, PAL and ROM. **[5M][L1][CO4]**
9. (a)Explain the architecture of PLA **[5M][L2][CO2]**
   (b)Briefly introduce the content addressable memory. **[5M][L1][CO2]**
10. Implement the following Boolean function using PAL. **[10M][L6][CO3]**
    (i)F1 (w,x,y,z) = Σm(0,1,2,3,7,9,11)
    (ii)F2 (w,x,y,z) = Σm(0,1,2,3,10,12,14)
    (iii)F3 (w,x,y,z) = Σm(0,1,2,3,10,13,15
    (iv)F4 (w,x,y,z) = Σm(4,5,6,7,9,15)
11. (a)Explain the 4X4 ROM construction with neat diagram. **[5M][L2][CO4]**
    (b) Implement NOT, NAND and NOR operation using CMOS logic **[5M][L2][CO4]**

UNIT –V
Essay (10 mark) Questions

1) a) Explain various data objects in VHDL. Give necessary examples. **[5M] [L2] [CO5]**

(b) Explain the structure of a VHDL program. **[5M] [L2] [CO5]**

2) Explain in detail different modeling styles of VHDL with suitable examples. **[10M] [L2] [CO5]**

3) Draw and explain in detail the VHDL design flow. **[10M] [L2] [CO5]**

4) a) Explain the importance of Schematic in VHDL. **[5M] [L1] [CO5]**

b) Explain about Data Types in VHDL. **[5M] [L2] [CO5]**

5) a) Write a VHDL program for a 4X1 MUX. **[5M] [L4] [CO5]**

b) Discuss in detail about Data Flow design elements. **[5M] [L4] [CO5]**

6) a) Design a logic circuit and write a VHDL program to add 3 bit numbers. **[5M] [L5] [CO5]**

b) Explain about Simulation and Synthesis processes in VHDL. [**5M] [L2] [CO5]**

7) Design the logic circuit and write a data-flow style VHDL program for the following function.

$F(A,B,C,D) = \sum (1,5,6,7,9,13) + d(4,15)$. **[10M] [L5] [CO5]**

8) a) Write about structural design elements with VHDL code. **[5M] [L1] [CO5]**

b) Write a VHDL entity and Architecture for the following function. F(x) = (a + b) (c d). Also draw the relevant logic diagram. **[5M] [L5]** [**CO5]**

9) a) Write a VHDL program for a 2 bit Magnitude Comparator using Data Flow model. **[5M] [L5] [CO5]**

b) Write a VHDL program for a D and T FF. **[5M] [L5] [CO5]**

10) a) Write a VHDL program for Full adder. [**5M] [L5] [CO5]**

b) Write a VHDL program for 3 to 8 Decoder. **[5M] [L5] [CO5]**

UNIT-I

Short (2 mark) Questions

1. Converting the following to octal: $(4243)_{16}$. (ii) $(125)_{10}$.
2. Express the given number (M=01000100) using 1's complement?
3. What is the need for taking complement?
4. Perform X-Y using 1's complement of the given binary numbers X = 1010100 and Y = 1000011.
5. Find 10's complement of given decimal numbers X = 52324 and Y =2421.
6. Why XS-3 code is called a self-complementing code?
7. What are the signed binary number systems?
8. What are the different classifications of binary codes?
9. State about error correcting codes?
10. What is meant by parity bit?
11. Define Demorgan's theorem.
12. Write the truth table for F=(A+B)(C+D)
13. State the associative law and commutative law.
14. State De Morgan's theorem and Duality.
15. Simplify the following expression Y = (A + B)(A '+ C)(B' + C')
16. Show that (X + Y' + XY)(X + Y')(X'Y) = 0
17. Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC
18. Define Canonical SOP & Canonical POS.
19. Define binary logic?
20. Define logic gates?

UNIT-II
Short (2 mark) Questions

1. Simplify the given Boolean function, F(X,Y,Z) = ∑(1,2,3,6,7).
2. Define Minterm and Maxterm.
3. Find the minterms of the given Boolean expressions
   $F=C^1D+AB\ C^1+ABD^1+A^1B^1D.$
4. Define Prime Implicant and Essential Prime Implicant.
5. Draw a 5 variable k-map.
6. Give the steps involved in analysis procedure for a combinational circuit.
7. Draw a Half Adder circuit and mention its truth table.
8. Draw a Half Subtractor circuit and mention its truth table.
9. Implement a Full Adder using Half Adders.
10. Mention the expressions for difference and borrow of Full Subtractor.
11. Draw the diagram of a 4 bit Binary Adder.
12. Draw the circuit of two bit by two bit binary multiplier.
13. Draw the 4*16 Decoder circuit using two 3x8 Decoders.
14. Define encoder and decoder.
15. Write the truth table of priority encoder.
16. List the applications of Encoder and Decoder.
17. Design a 2:1 Multiplexer.
18. Define Mux and Demux.
19. List the applications of MUX and DEMUX.
20. Define Carry Look Ahead Adder.

UNIT-III
Short (2 mark) Questions

1. Write the difference between Latch and Flip flop
2. Briefly explain about D-FF
3. Draw the block diagram of sequential circuit using combinational circuit and memory unit
4. Draw the logic circuit of flip-flop and truth table using NAND gates
5. Give the comparison between combinational circuits and sequential circuits
6. What is shift register? Give the classification of them?
7. Draw the circuit of ring counter.
8. What is the operation of SR flip-flop?
9. What are the different types of flip-flop?
10. Define Flip flop. What are the applications of FF
11. What is the operation of JK flip-flop?
12. Draw the PIPO shift register
13. What is edge-triggered flip-flop?
14. What are different types of counter
15. Explain the flip-flop excitation tables for JK flip-flop
16. Draw the MOD-2 Counter.
17. Draw the SIPO shift register
18. Give the comparison between synchronous & Asynchronous counters.
19. What is a master-slave flip-flop?
20. What are the classifications of sequential circuits?

UNIT-IV
Short (2 mark) Questions

1. Define Propagation delay and Fan-out.
2. Draw the symbol of NMOS and PMOS transistor.
3. Define noise margin.
4. Draw CMOS AND gate.
5. What are the advantages of flash memory?
6. Draw the DTL OR gate.
7. What is the concept of ROM?
8. What are the advantages of PLDs.
9. List different PLDs.
10. Draw CMOS OR gate.
11. Draw the structure of PAL.
12. What is meant by Tristate TTL
13. Compare PAL, PLA & PROM.
14. Realize $F(x,y,z) = \Sigma m(1,2,5,7)$ using PLA.
15. Realize $F(x,y,z) = \Sigma m(1,2,3,6)$ using PAL
16. How does the PLDs differ from fixed logic devices?
17. Find the number of address lines to access 4KB ROM.
18. What is static memory?
19. List the differences between static & dynamic memories.

UNIT-V

Short (2 mark) Questions

1. List the different objects of VHDL.
2. Define FSM.
3. What is the need of HDL?
4. Give the difference between Signal and Variable.
5. Give any two differences between different modeling styles of VHDL.
6. Define Data flow model.
7. Define Structural model.
8. Define Behavioral model.
9. State the basic statement used in behavioral Modeling.
10. Define Process and Sequential Statements with example.
11. Write an entity declaration for 1x8 De-Mux.
12. Write a VHDL Program for 1x4 DEMUX in Dataflow Model.
13. Write a VHDL Program for Half adder in Structural Model.
14. Write a VHDL Program for Full adder in Behavioral Model.
15. Write a VHDL Program for 1x8 De-MUX in Structural Model.
16. Write a VHDL Program for Half Subtractor in Dataflow Model.
17. Write a VHDL Program for Full Subtractor in Structural Model.
18. Write a VHDL Program for 2x4 Decoder in Dataflow Model.
19. Write a VHDL Program for 4x2 Encoder in Structural Model.
20. Write an Entity Declaration for 4x8 Decoder in Structural Model.